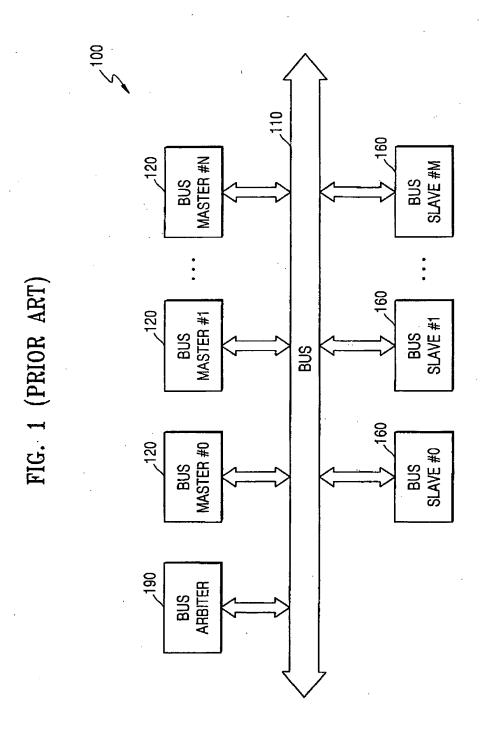
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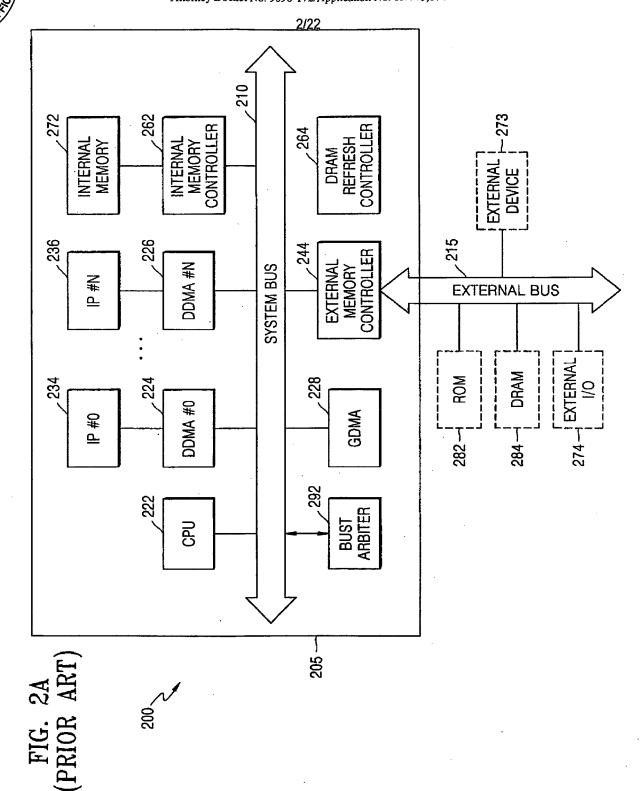
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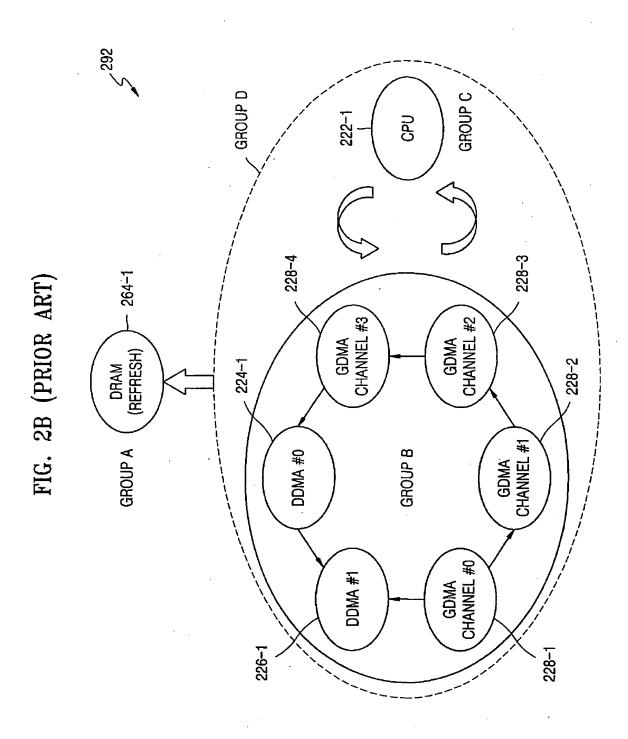


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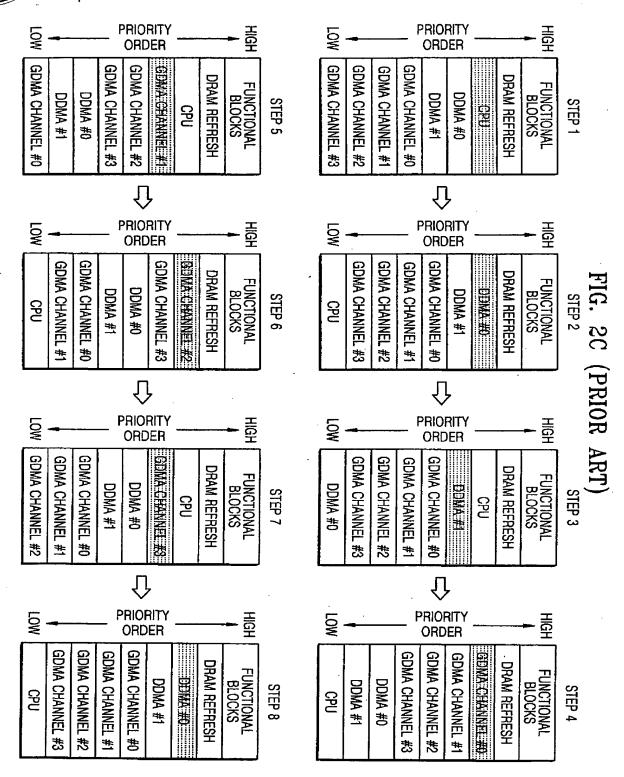
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FOR BOTH BUSES, SOFTWARE, AND METHOD FOR ASSIGNING PROGRAMMABLE PRIORITIES

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5/22 210 273 CONTROLLER MEMORY MEMORY NTERNAL INTERNAL 315 EXTERNAL MEMORY CONTROLLER BUS DDMA #N ₹ **EXTERNAL BUS** SYSTEM <u>\_</u> EXTERNAL 1/0 **BUS ARBITER** DRAM EXTERNAL S DDMA #0 **GDMA** 9 <u>a</u> 282 284 274 396 SYSTEM BUS ARBITER S

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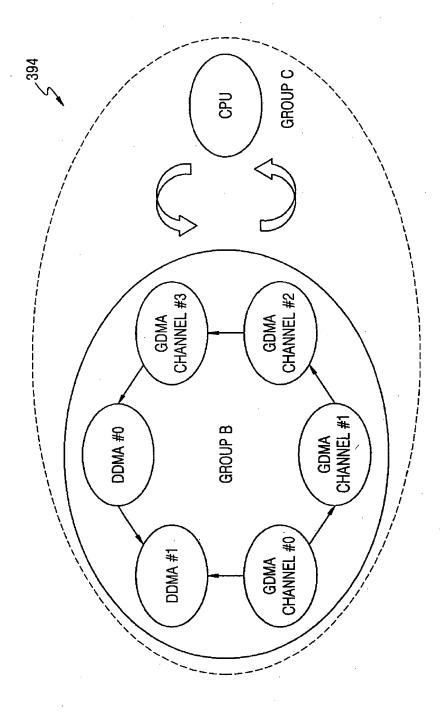
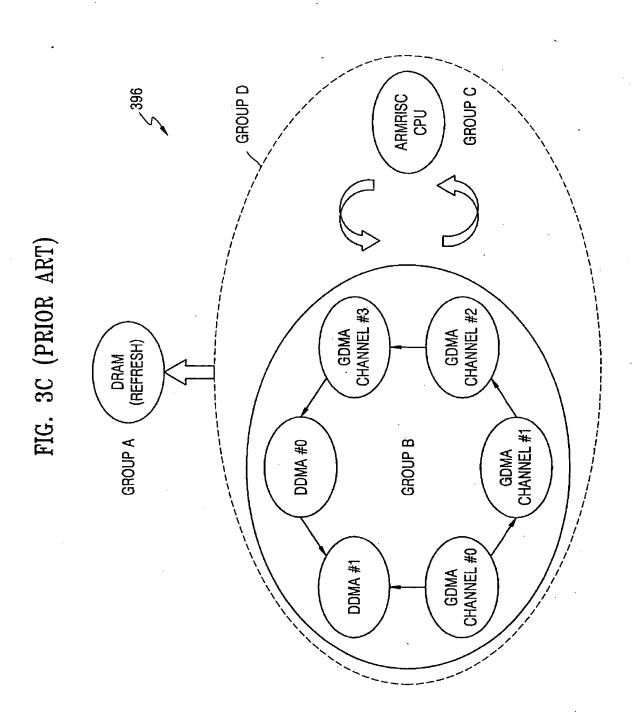


FIG. 3B (PRIOR ART)



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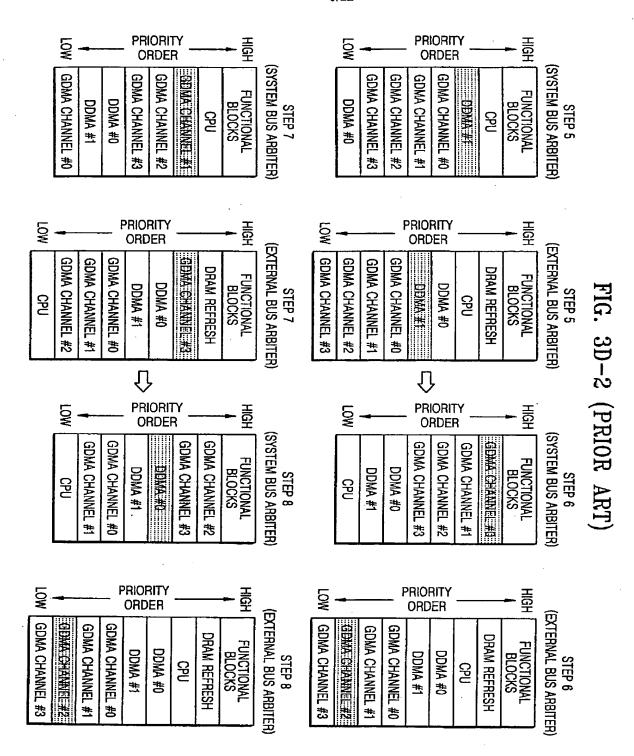
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8/22 PRIORITY HGH **PRIORITY** 퍞 ᅙ ORDER **ORDER** (SYSTEM BUS ARBITER) (SYSTEM BUS ARBITER) **GDMA CHANNEL #3 GDMA CHANNEL** GDMA CHANNEL #3 **GDMA CHANNEL #2 GDMA CHANNEL #1** GDMA CHANNEL #0 **GDMA CHANNEL #2** GDMA CHANNEL #1 FUNCTIONAL BLOCKS **FUNCTIONAL** DDMA #1 DIMA#O DDMA #0 DDMA #1 CPU 윧 되었 픞 **PRIORITY PRIORITY** Ş Ş 8 **ORDER** ORDER (EXTERNAL BUS ARBITER) (EXTERNAL BUS ARBITER) **GDMA CHANNEL #3 GDMA CHANNEL #2** GDMA CHANNEL GDMA CHANNEL # GDMA CHANNEL #0 GDMA CHANNEL #3 GDMA CHANNEL #1 GDMA CHANNEL #0 DRAM REFRESH FUNCTIONAL BLOCKS DRAM REFRESH FUNCTIONAL DDMA #1 DDMA #1 DDWA #0 DDMA #0 STEP 3 원 Û  $\hat{\Omega}$ PRIORITY ORDER PRIORITY 표 퍒 MO 8 PRIOR ART **ORDER** (SYSTEM BUS ARBITER) (SYSTEM BUS ARBITER) GDMA CHANNEL GDMA CHANNEL #2 GDMA CHANNEL GDMA CHANNEL GDMA CHANNEL GDMA CHANNEL #0 3DMA CHANNEL 3DMA CHANNEL #2 FUNCTIONAL BLOCKS FUNCTIONAL BLOCKS DDMA #0 DDMA #1 DEMAKED E TH AMOL 원 윧 톺 된으로 **PRIORITY PRIORITY** Ş **ORDER ORDER** (EXTERNAL BUS ARBITER) Step 2 (External bus arbiter) **GDMA CHANNEL #3** GDMA CHANNEL #0 GDMA CHANNEL #2 GDMA CHANNEL GDMA CHANNEL GDMA CHANNEL #1 DMA CHAMIEL #2 FUNCTIONAL BLOCKS FUNCTIONAL BLOCKS DRAM REFRESH DRAM REFRESH DDMA #1 STEP 4 DDMA #0 DDMA #0 DDMA #1 원 පි

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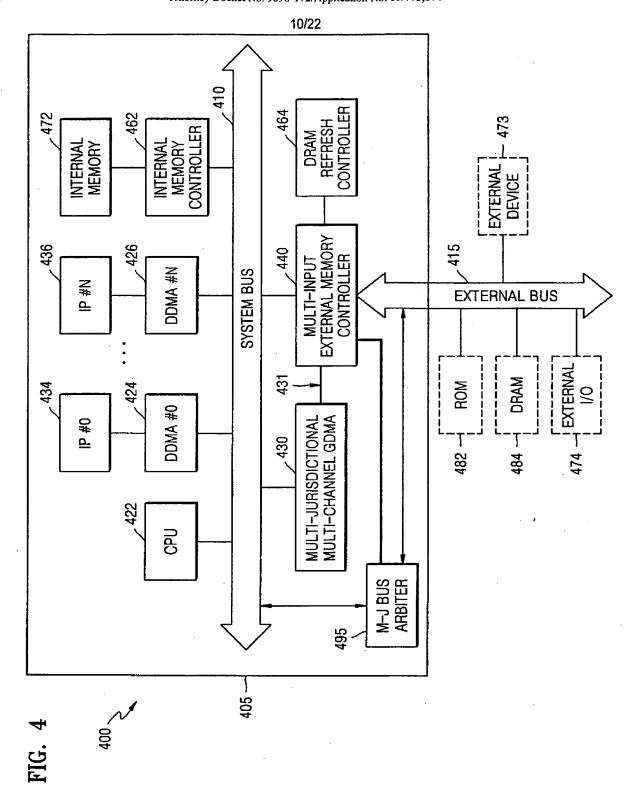
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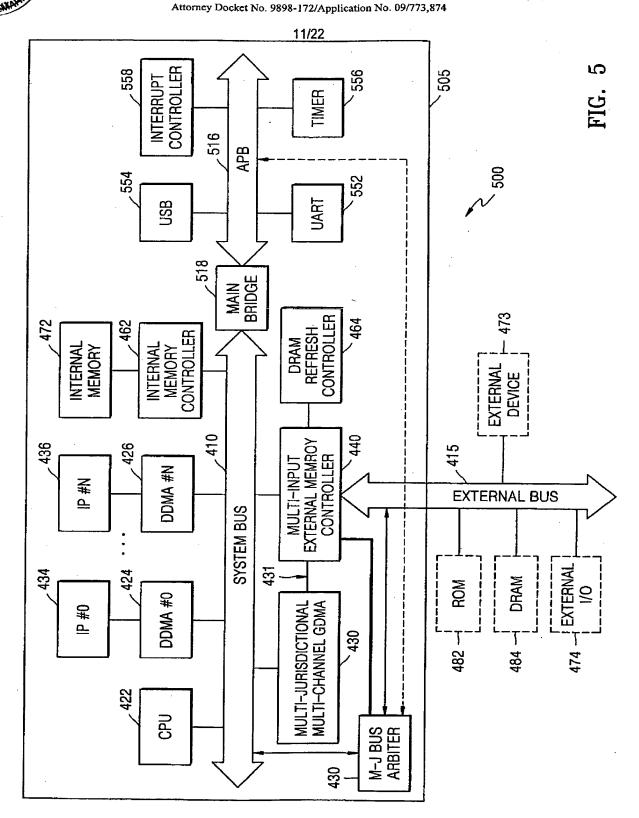
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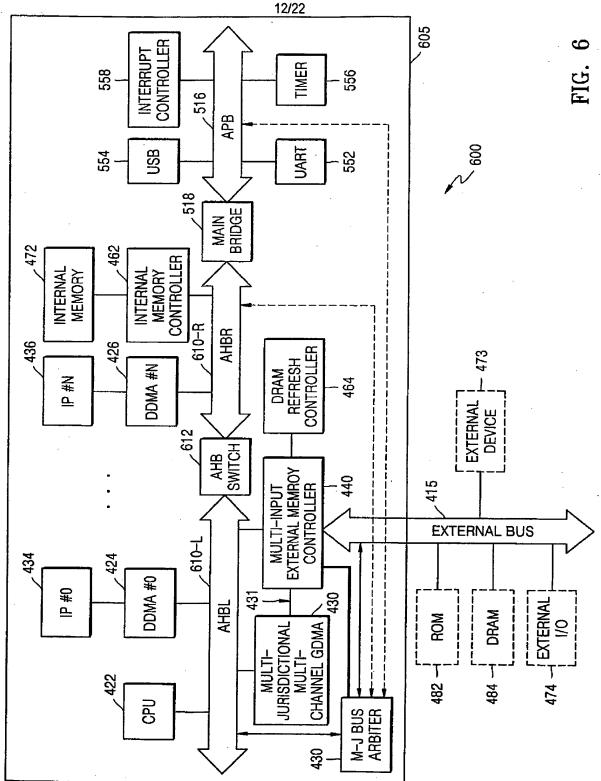
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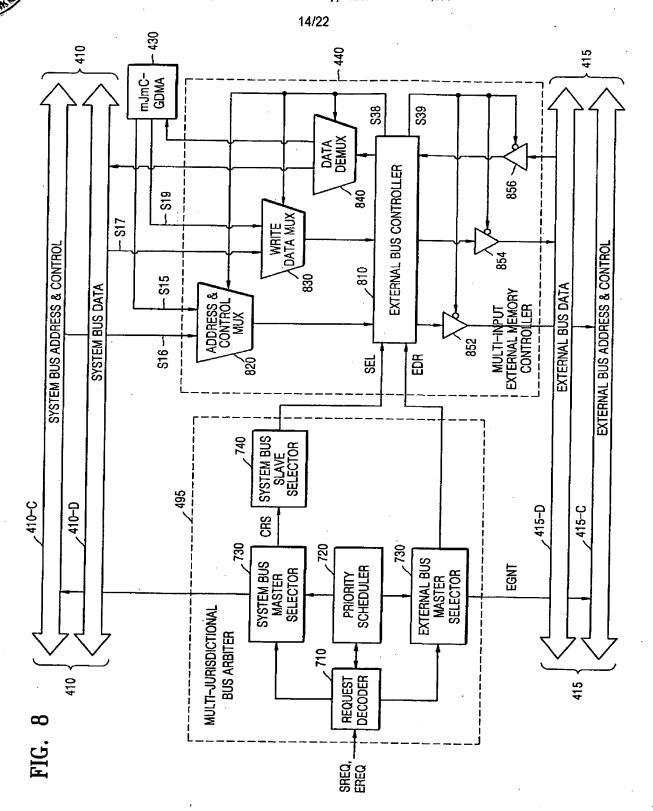
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13/22 SYSTEM BUST DATA SYSTEM BUST DATA ADDRESS AND CONTROL က S S18 **EXTERNAL** MEMORY CONTROLL SE SYSTEM BUS SELECTOR EDR CRS 330 EXTERNAL BUS MASTER SYSTEM BUS MASTER SELECTOR SCHEDULEF SELECTOR PRIORITY MULTI-JURISDICTIONAL **BUS ARBITER** DECODER REQUEST

THE THE BEMAN

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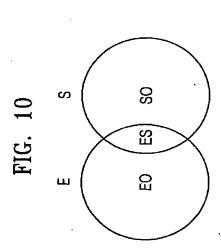
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		EXTERNAL BUS MASTER	SYSTEM BL MASTER	SYSTEM BUS MASTER
	NO REQUEST REQ[1:0]=2' b00	EXTERNAL BUS ONLY REQ[1:0]=2' b10	SYSTEM BUS ONLY REQ[1:0]=2' b01	BOTH BUSES REQ[1:0]=2' b11
DRAM REFRESH CONTROLLER	0	0	×	×
CPU	0	×	0	0
DDMA BLOCK	0	×	0	0
GDMA CHANNEL	0	0	0	0
EXTERNAL DEVICE	0	0	×	×



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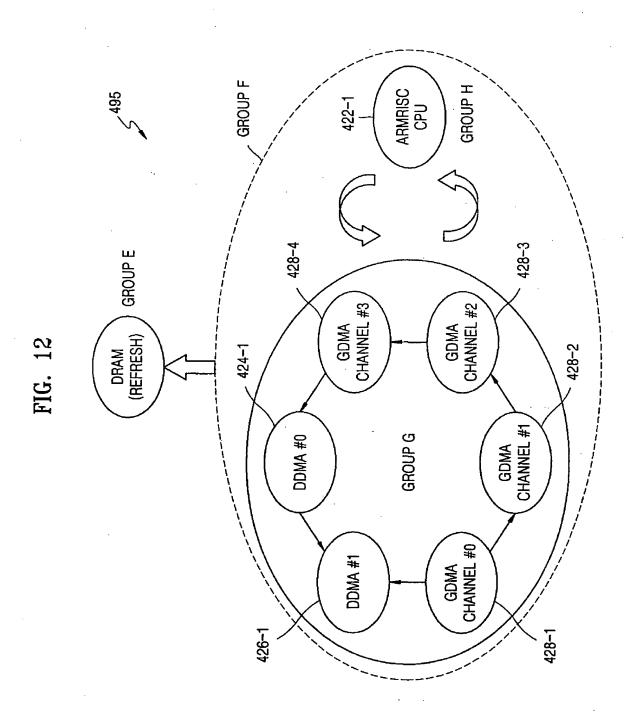
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CLASSIFICATION OF SET	ELEMENT
SET OF FUNCTIONAL BLOCKS MAKING A SYSTEM BUS REQUEST (SYSTEM BUS MASTER S)	CPU, DDMA BLOCK, AND GDMA BLOCK
SET OF FUNCTIONAL BLOCKS MAKING AN EXTERNAL BUS REQUEST (E)	DRAM REFRESH CONTROLLER, CPU, DDMA BLOCK, GDMA CHANNEL, AND EXTERNAL DEVICE
SET OF FUNCTIONAL BLOCKS MAKING ONLY A SYSTEM BUS REQUEST (SO)	СРU
SET OF FUNCTIONAL BLOCKS MAKING ONLY AN EXTERNAL BUS REQUEST (EO)	DRAM REFRESH CONTROLLER, GDMA CHANNEL, AND EXTERNAL DEVICE
SET OF FUNCTIONAL BLOCKS MAKING A REQUEST FOR BOTH SYSTEM BUS AND EXTERNAL BUS (ES)	CPU, DDMA BLOCK, AND GDMA CHANNEL
SET OF FUNCTIONAL BLOCKS MAKING REQUESTS FOR A SYSTEM BUS OR AN EXTERNAL BUS (A)	DRAM REFRESH CONTROLLER, CPU, DDMA BLOCK, GDMA CHANNEL, AND EXTERNAL DEVICE

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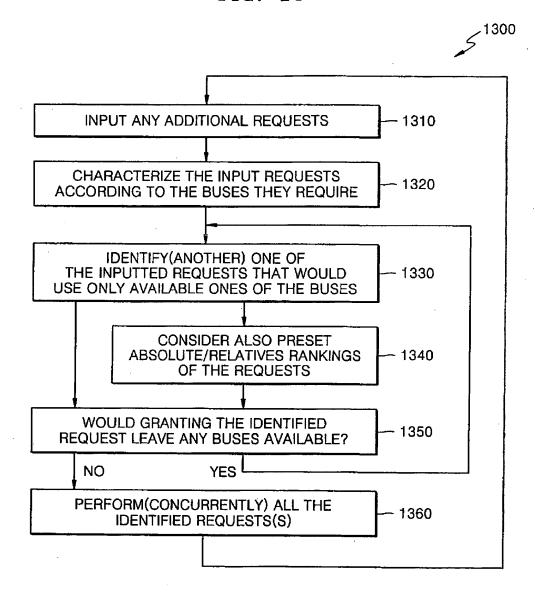
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FIG. 13



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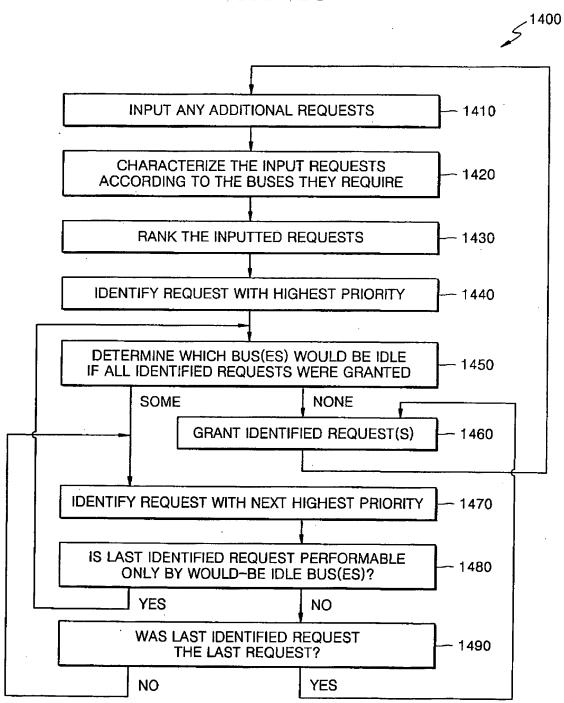
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FIG. 14

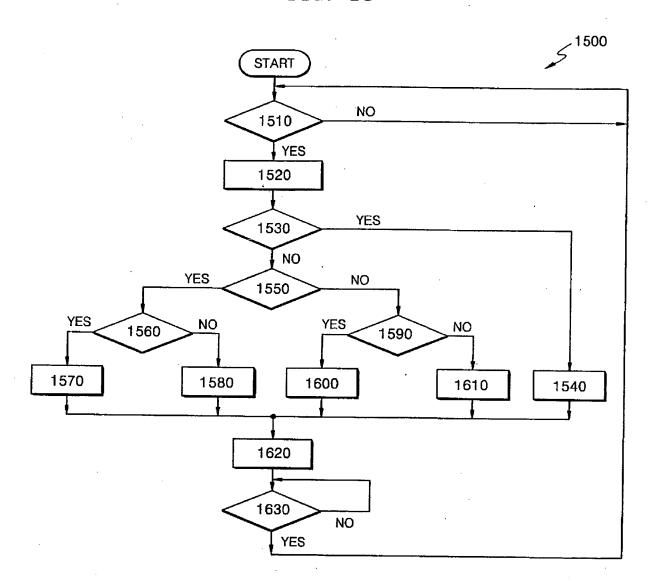


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FIG. 15



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	LOW				PRIC OR	DER	Υ		<del>~</del> 턆		LOW			_ '	PRIO ORI				<del></del> 률		
	GDMA CHANNEL #1	GDMA CHANNEL #0	DDMA #1	DDMA #0	ODWA CHANNEL#3	GDWAY CHANNEL #2 12 bij	CPU	DRAM REFRESH	FUNCTIONAL BLOCKS	STEP 5	GDMA CHANNEL #3	GDMA CHANNEL #2	GDMA CHANNEL #1	GDMA CHANNEL #0	DDMA #1	DDMA #0		DRAM REFRESH	FUNCTIONAL BLOCKS	STEP 1	
	2'601	2'b10	2'b11	2'b11	2 501	2010	2,900	2,900	贾		2'b10	2'b10	2'b01	2'501	2'b11	2'511	2511	2'b00	殿		
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	CPU	GDMA CHANNEL #3	GDMA CHANNEL #2	GDMA CHANNEL #1	GDMA CHANNEL #0	DDMA #1	DD####0	DRAM REFRESH	FUNCTIONAL BLOCKS	STEP 6	CPU	GDMA CHANNEL #3	GDMA CHANNEL #2	GDMA CHANNEL #1	GDMA CHANNEL #0	DDMA #1	DDWA#0	DRAM REFRESH	FUNCTIONAL BLOCKS	STEP 2	
	2'b00	2'b01	2'b10	2'b01	2'510	2 <sup>b</sup> 11	261	2'b00	REQ		2'600	2'b10	2'510	2'b01	2'501	2'511	251	2'500	RED		اعدا
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	<u>چ</u>			F	PRIO.		·		프		_			P	RIOF	RITY			_		16
	₹				ORD	ER			<del>-</del> 돌		₩ V	_			ORD	ER			~ 호		ത
	W DDMA #0	GDMA CHANNEL #3	GDMA CHANNEL #2	GDMA CHANNEL #1		ER DDWA#	СРИ	DRAM REFRESH	GH FUNCTIONAL BLOCKS	STEP 7	OW DDMA #0	GDMA CHANNEL #3	GDMA CHANNEL #2	GDMA CHANNEL #1	ORD	E DIM #	СРИ	DRAM REFRESH	HIGH FUNCTIONAL BLOCKS	STEP 3	G
	DDMA #0	GDMA CHANNEL #3 2'b01	GDMA CHANNEL #2 2'b10	GDMA CHANNEL #1 2'b01	ORD		CPU 2'b00	DRAM REFRESH 2'b00		STEP 7		GDMA CHANNEL #3 2'b10	GDMA CHANNEL #2 2'b10	GDMA CHANNEL #1	GDMA CHANNEL #0	ER	CPU 2'b00			STEP 3	G
	DDMA #0				GDMA CHANNEL #0	DDWA#!			FUNCTIONAL BLOCKS	STEP 7	DDMA #0			GDMA CHANNEL #1	GDMA CHANNEL #0 2'b01 C			DRAM REFRESH 2'b00	FUNCTIONAL BLOCKS	STEP 3	6
	DDMA #0			2'b01	GDMA CHANNEL #0				FUNCTIONAL BLOCKS	STEP 7	DDMA #0			GDMA CHANNEL #1 2'b01	GDMA CHANNEL #0	65			FUNCTIONAL BLOCKS	STEP 3	6
	DDMA #0 2'b11 (OW CPI)	2'b01	2'b10	2'b01 GDMA CHANNEL #3	GDMA CHANNEL #0 2'b10 다 함요			2'600	FUNCTIONAL REQ	STEP 7 STEP 8	DDWA #0 2'b11		2'b10	GDMA CHANNEL #1 2'b01	GDMA CHANNEL #0 2'b01 RORD	氏 DDM# Zbit ER		21500	FUNCTIONAL REQ	STEP 3 STEP 4	6

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		22/22		
BUS UTILIZATION		n(EO)+2n(EO)+n(SO) 2n(A)	4n(SO)+3n(ES) 4n(S)	
VING BUS JATION	ELEMENT OF SET SO	1 n(A)	n(A)	n(EO)+n(SO) n(A)n(SO)
PROBABILITY THAT ELEMENT HAVING BUS OWNERSHIP PERFORMS OPERATION	ELEMENT OF SET ES	1 n(A)	1 2n(S)	1 n(A)
PROBABI	ELEMENT OF SET EO	1 n(A)	n(ES)+2n(SO) 2n(S)n(EO)	n(EO)+n(SO) n(A)n(EO)
ITEM		EXCLUSIVE BUS ARBITRATION	HIERACHICAL BUS ARBITRATION	PRESENT INVENTION